## REMARKS

Reconsideration of this application, as amended, is respectfully requested. Claims 1-69 remain pending. Claims 1-69 have been rejected.

Claims 1 and 34 have been amended. No claims have been cancelled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

## REJECTIONS UNDER 35 U.S.C. § 102

Claims 1-2, 4-7, 9-20, 23-30, 32-35, 37-40, 42-53, 56-63, 65-66 and 68 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,446,198 to Sazegari ("Sazegari").

Applicants have amended claim 1 to include selecting a plurality of segments of bits from the string of bits. A plurality of indices is generated using the plurality of selected segments of bits from this string of bits.

Sazegari discloses a table look-up using a permute instruction. More specifically, Sazegari discloses

> In a vectorized processing unit, one approach that has been employed to perform multiple simultaneous table lookups is through the use of the "permute" instruction. This instruction operates to fill a register with data values from two other registers. The data values can be specified in any order. Referring to FIG. 3, a permute mask is stored in a register 26, and values that are to be used to form the final result are stored in two data registers 28 and 30. The permute instruction uses the mask values in the register 26 to assign corresponding values of the operands in the registers 28 and 30 to a result register 32. In the illustrated example, byte(1) of register 28 is mapped to byte(0) of the result register, and byte(14) of register 30 is mapped to byte(1) of the result register. In this example, each of the registers stores 16 bytes, i.e. 128 bits. The permute instruction therefore enables any one of 32 source bytes, i.e. the 16 bytes of the vectors stored in each of the two registers 28 and 30, to be mapped to any location within the destination vector stored in the register 32.
>
> (Sazegari, col. 4, lines 5-23) ( emphasis added)

In particular, Sazegari discloses

For table lookup operations, the permute instruction can be used to perform 16 simultaneous lookup operations on a 32-byte entry table. FIG. 4 illustrates such a table 34, which consists of two 16-byte vectors, data1 and data2. Each vector can be stored in one register of the CPU. The permute instruction can be used to simultaneously read 16 values from these two vectors, in accordance with index values in a register 36, and store the 16 output results in sequential order in another register 38.

(Sazegari, col. 4, lines 24-32) (emphasis added)

Thus, Sazegari merely discloses providing indexes into a look-up table using mask values stored in a register. In contrast, amended claim 1 refers to selecting a plurality of segments of bits from the string of bits, and generating a plurality of indices using the plurality of selected segments of bits from the string of bits.

Because Sazegari fails to disclose all limitations of amended claim1, applicants respectfully submit that amended claim 1 is not anticipated by Sazegari under 35 U.S.C. § 102(e).

Given that claims 2, 4-7, 9-20, 23-30, 32-35, 37-40, 42-53, 56-63, 65-66 and 68 contain related limitations, applicants respectfully submit that claims 2, 4-7, 9-20, 23-30, 32-35, 37-40, 42-53, 56-63, 65-66 and 68 are not anticipated by Sazegari under 35 U.S.C. 102§(e).

## REJECTIONS UNDER 35 U.S.C. § 103

Claims 3, 8, 21-22, 31, 36, 41, 54-55, 64 and 69 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Sazegari, as applied above.

As set forth above, Sazegari merely discloses providing indexes into a look-up table using mask values stored in a register, and fails to disclose, teach, or suggest selecting a plurality of segments of bits from the string of bits, and generating a plurality of indices using the plurality of selected segments of bits from the string of bits, as recited in amended claim 1.

Given that claims 3, 8, 21-22, 31, 36, 41, 54-55, 64 and 69 contain related limitations, applicants respectfully submit that claims 3, 8, 21-22, 31, 36, 41, 54-55, 64 and 69 are not obvious are not obvious under 35 U.S.C. § 103(a) over Sazegari.

Claim 67 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Sazegari, as applied above, in view of U.S. Patent No. 5,526,501 to Shams ("Shams").

Shams, in contrast, discloses accessing the look-up tables by the array of processors, and similarly to Sazegari, fails to disclose, teach, or suggest selecting a plurality of segments of bits from the string of bits, and generating a plurality of indices using the plurality of selected segments of bits from the string of bits, as recited in amended claim 1.

Given that claim 67 depends from amended claim 1, and add additional limitations, applicants respectfully submit that claim 67 is not obvious under 35 U.S.C. § 103(a) over Sazegari in view of Shams.

## CONCLUSION

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 2/21/2007

By: _____
James C. Scheller
Reg. No.: 31,195

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(408) 720-8300
Fax (408) 720-8383